

R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

The present invention concerns an apparatus generally comprising a low speed tester and a host emulator. The host emulator may have (i) a first interface coupled to the low speed tester to receive a test vector at a first speed, (ii) a second interface configured to (a) transmit the test vector to a device at a second speed faster than the first speed and (b) receive a response from the device and (iii) a third interface to the low speed tester to transfer a signal based upon the response, wherein the apparatus is configured to allow the low speed tester to perform high speed tests of the device at the second speed.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 1-20 under 35 U.S.C. §103(a) as being unpatentable over "SBAE-10 Bus Analyzer-Exerciser User's Manual" and "Analyzer/Exercise/Tester" specification sheet, both by Catalyst Enterprises, Inc. (hereafter Catalyst) in view of Goutzoulis et al. '630 (hereafter Goutzoulis) is respectfully traversed and should be withdrawn.

Catalyst concerns a bus analyzer/exerciser/tester system. Goutzoulis concerns a method and apparatus for generating and transferring high speed data for high speed testing applications

(Title). Catalyst and Goutzoulis, alone or in combination, do not appear to teach or suggest every element as presently claimed. Furthermore, *prima facie* obviousness has not been established for a lack of motivation of combine and/or a lack of a reasonable expectation of success. As such the claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

"[T]o establish obviousness based on a combination of the elements disclosed in the prior art, there must be some motivation, suggestion or teaching of the desirability of making the specific combination that was made by the applicants."¹ "[T]he factual inquiry whether to combine references must be thorough and searching."² "This factual question ... [cannot] be resolved on subjective belief and unknown authority."³ "It must be based on objective evidence of record."⁴ The Examiner must show that (a) there is some suggestion or motivation, either in the references or in the knowledge generally available to one of ordinary skill in the art, to modify or combine the references, (b) there is a

¹ *In re Kotzab*, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1316 (Fed. Cir. 2000) (citing *In re Dance*, 160 F.3d 1339, 1343, 48 USPQ2d 1635, 1637 (Fed. Cir. 1998); *In re Gordon*, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984)).

² *McGinley v. Franklin Sports, Inc.*, 262 F.3d 1339, 1351-52, 60 USPQ2d 1001, 1008 (Fed. Cir. 2001).

³ *In re Lee*, 277 F.3d 1338, 1343-44, 61 USPQ2d 1430, 1434 (Fed. Cir. 2002).

⁴ *Id.* at 1343, 61 USPQ2d at 1434.

reasonable expectation of success, and (c) the prior art reference (or combination of references) teaches or suggests all of the claim limitations as arranged in the claims.⁵ Furthermore, The Court of Appeals for the Federal Circuit has indicated that the requirement for showing the teaching of motivation to combine references is "rigorous" and must be "clear and particular".⁶

Claim 1 provides a host emulator having (i) a first interface coupled to a low speed tester to receive a test vector at a first speed and (ii) a second interface configured to transmit the test vector to a device at a second speed faster than the first speed. Page 3, line 16 thru page 4, line 3 of the Office Action appear to assert that it would have been obvious to combine Goutzoulis with Catalyst to cause a first USB between a personal computer (PC) and a host SBAE-10 device of Catalyst to operate at a first speed and a second USB between the host SBAE-10 device and an exercised SBAE-10 device of Catalyst to operate at a second speed faster than the first speed. However, the Office Action fails to state if the modification slows the first speed for the first USB and/or increases the second speed for the second USB.

Assuming, *arguendo*, that the proposed modification slows the first speed, no motivation appears to exist to modify Catalyst.

⁵ Manual of Patent Examining Procedure (M.P.E.P.), Eighth Edition, Revised February 2003, §2142.

⁶ *In re Anita Dembiczak and Benson Zinbarg*, 50 U.S.P.Q.2d 1614 (Fed. Cir. 1999)

In particular, one of ordinary skill in the art would have no realistic motivation for adding the complexity of Goutzoulis to Catalyst to intentionally decrease a performance of the first USB between the PC and the host SBAE-10 device. The fact that references can be combined or modified is not sufficient to establish *prima facie* obviousness.⁷ Therefore, no motivation appears to exist to slow the first USB.

Assuming, *arguendo*, that the proposed modification increases the second speed, no reasonable expectation of success appears to exist. In particular, Goutzoulis appears to teach how to convert a parallel signal loaded in a memory 10 to a serial signal transferrable to a device under test (DUT) 28 at high-speed. Therefore, the proposed modified host SBAE-10 device may be capable of transfer data on the second USB at a speed (i.e., high-speed) faster than the data was received via the first USB. Since the host SBAE-10 device was modified to transmit at high-speed, the exercised SBAE-10 device would also have to be modified to receive at high-speed. However, both Catalyst and Goutzoulis are silent regarding how to modify the exercised SBAE-10 device to receive the high-speed serial signal. Therefore, the proposed modification does not appear to have a reasonable expectation of success because (i) an unmodified exercised SBAE-10 device does not appear to be capable of receiving the high-speed signal and (ii) no obvious

⁷ M.P.E.P., Eighth Edition, Revised February 2003, §1243.01.

modification has been cited in the Office Action to provide a high-speed reception capability. As such, *prima facie* obviousness has not been established for the claimed invention.

Claim 1 further provides the host emulator having (ii) a second interface configured to (a) transmit a test vector to a device and (b) receive a response from the device. In contrast, Goutzoulis appears to teach that the conversion from a low-speed parallel signal to high-speed serial signal produces a unidirectional interface. In particular, an optoelectronic converter 26 used by Goutzoulis to present the high-speed signal in electrical form to the DUT 28 does not appear to be capable of receiving an electronic signal back from the DUT 28. Therefore, Catalyst and Goutzoulis, alone or in combination, do not appear to teach or suggest a host emulator having (ii) a second interface configured to (a) transmit a test vector to a device and (b) receive a response from the device as presently claimed. Claims 15 and 16 provide language similar to claim 1. As such, the claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

Claim 3 depends from the claim 1 and thus contains all of the limitations of the claim 1. Consequently, the arguments presented above in support of the patentability of claim 1 are incorporated hereunder in support of claim 3.

Claim 3 further provides that a device (being tested) comprises a Universal Serial Bus (USB) device. As argued above for claim 1, no motivation appears to exist to slow the first USB between the PC and host SBAE-10 device of Catalyst. If Catalyst is modified to increase the speed of the second USB, then both the host SBAE-10 device and the exercised SBAE-10 device would be communicating with each other outside of the USB specification. An exercised SBAE-10 device modified to communicate at high-speed using "ultrashort picosecond-type pulses" (Goutzoulis column 2, lines 28-29) does not appear to be USB compliant. Therefore, Catalyst and Goutzoulis, alone or in combination, do not appear to teach or suggest a device comprising a Universal Serial Bus (USB) device as presently claimed. Claim 17 provides language similar to claim 3. As such, claims 3 and 17 are fully patentable over the cited references and the rejection should be withdrawn.

Claim 7 depends indirectly from the claim 1 and thus contains all of the limitations of the claim 7. Consequently, the arguments presented above in support of the patentability of claim 1 are incorporated hereunder in support of claim 7.

Claim 7 further provides a test vector generator configured to generate a test vector. In contrast, Goutzoulis appears to be silent regarding a test vector generator for generating the data stored in the memory 10. Catalyst appears to allocate test vector generation to a user and/or PC (asserted to be

similar to the claimed low speed tester but not the claimed test vector generator). Therefore, Catalyst and Goutzoulis, alone or in combination do not appear to teach or suggest a test vector generator (independent of a low speed tester) configured to generate a test vector as presently claimed.

Claim 7 further provides (from claim 4) that the test vector generator transfers the test vector to a low speed tester. Assuming, *arguendo*, that Goutzoulis somehow teaches a test vector generator, (for which Applicants' representative does not necessarily agree), Goutzoulis does not appear to present the test data stored in the memory 10 in a format suitable for a low speed tester. In particular, FIGS. 1 and 3 of Goutzoulis appear to transfer the test data directly to the DUT 28 at high-speed. Even if the test data were routed to a low speed tester, no reasonable expectation of success appears to exist for the low speed tester to properly receive the high-speed test data. Therefore, Catalyst and Goutzoulis, alone or in combination, do not appear to teach or suggest that a test vector generator transfers a test vector to a low speed tester as presently claimed. As such, claim 7 is fully patentable over the cited references and the rejection should be withdrawn.

Claim 13 depends from the claim 1 and thus contains all of the limitations of the claim 1. Consequently, the arguments

presented above in support of the patentability of claim 1 are incorporated hereunder in support of claim 13.

Claim 13 further provides a low speed tester configured to generate a pass/fail signal. In contrast, page 5, lines 12-14 of the Office Action state that Catalyst provides a pass/fail signal in the Specification Sheet, page 1, column 1 and in the User's Manual, page 2. Page 1, column 1 of the Specification Sheet appears to be silent regarding a pass/fail signal. Page 2 of the User's Manual indicates that the host SBAE-10 device may generate a pass/fail signal for a current inrush test. However, the Office Action appears to consider the host SBAE-10 device to be similar to the claimed host emulator. Thus, Catalyst appears to allocate generation of a pass/fail signal to the wrong claim element. Therefore, Catalyst and Goutzoulis, alone or in combination, do not appear to teach or suggest a low speed tester configured to generate a pass/fail signal as presently claimed.

Furthermore, the assertion on page 5, lines 9-10 of the Office Action that a user may decide pass or fail from the data displayed on the PC is moot since a user is not part of the circuit. As such, claim 13 is fully patentable over the cited references and the rejection should be withdrawn.

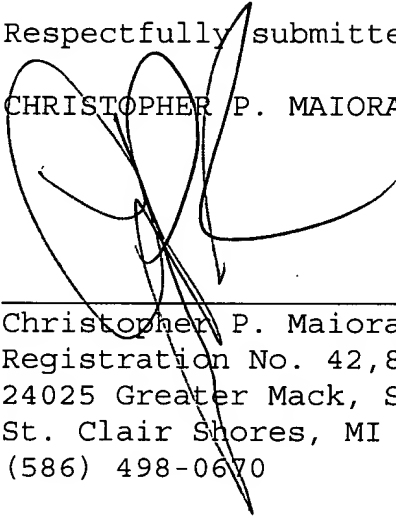
Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

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